PCB Layout and Design Guide for CH7517

DispalyPort to VGA Converter

1.0 INTRODUCTION

This application note focuses only on the basic PCB layout and design guidelines for CH7517. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 40-pin QFN (5x5 mm) package of the CH7517. Please refer to the CH7517 datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7517 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7517 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The CH7517 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7517 ground pins should be connected to its respective decoupling capacitor ground lead directly, and then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7517 (QFN40)

Pin Assignment	# of Pins	Type	Symbol	Description
11,37	2	Power	DVDD	Digital supply voltage (1.2V)
33	1	Power	AVDD	Analog supply voltage (1.2V)
10	1	Power	VDD_PLL	PLL supply voltage (1.2V)
6,18	2	Power	AVCC	Analog supply voltage (3.3V)
23,27	2	Power	AVCC_DAC	DAC supply voltage (3.3V)
12,36	2	Ground	DGND	Digital supply ground
30	1	Ground	AGND	Analog supply ground

9	1	Ground	GNDPLL	PLL supply ground
5,17,25,29	4	Ground	AVSS	Analog supply ground

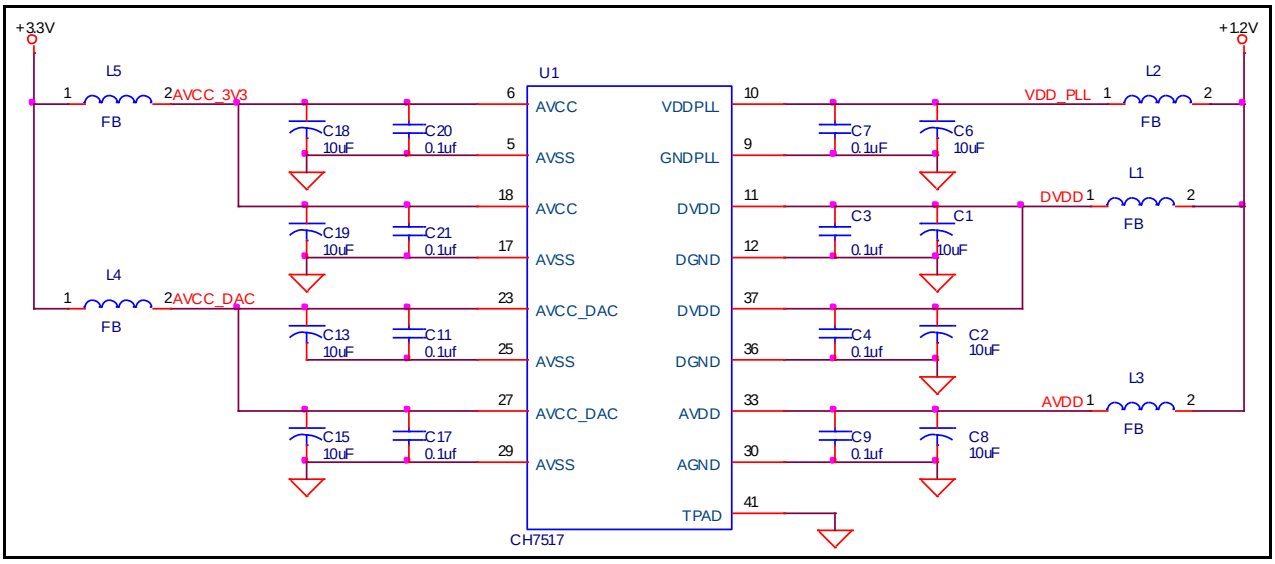

Figure 1: Power Supply Decoupling and Distribution

2.2 Power On and Reset

RSTB pin is the chip reset pin for CH7517. RSTB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low.

There are two methods for chip power-on reset.

1. The RB signal can be generated by on board Resistor and Capacitor delay, which can be refer to Figure 4.

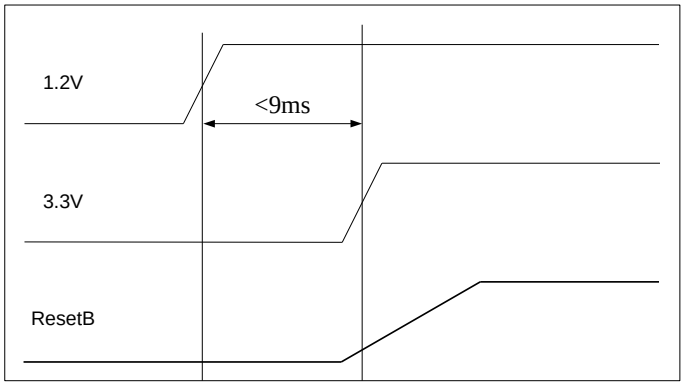

Figure 2: Power-on Reset Function's Sequence on board

Please note that the 1.2V power should be rise-up no later than the 3.3V power. Refer to Figure 2.

2. RB signal is generate by system global reset. In this case, the power supply should be valid and stable for at least 20ms before the reset signal is valid. The pulse width of valid reset signal should be at least 100us. Otherwise, the chip can't work well. The timing is shown in Figure 3.

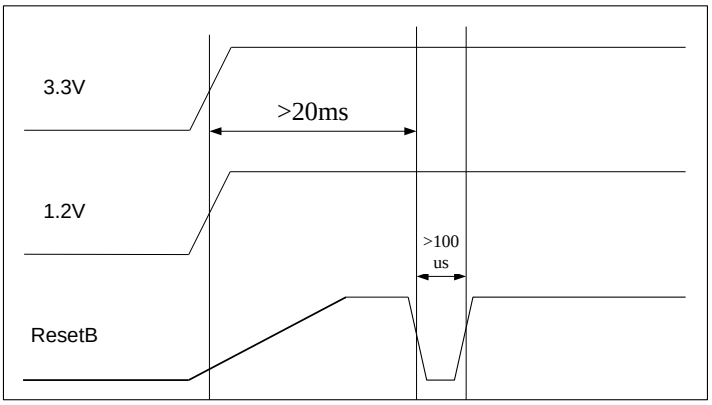

Figure 3: Power-on Reset Function's Sequence external global reset

Note:

1. The power supply will be valid when it rises to 90% of standard level.
2. The rising time of power supply should not exceed 2.5ms.
3. The rising threshold of RSTB is 2.4V.
4. The falling threshold of RSTB is 0.4V.

2.3 Internal Reference Pins

• RBIAS pin

This pin sets the Band-gap Bias Voltage. A 10 K-Ohm, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure** 4. A smaller resistance will create less Band-gap Bias voltage. This resistor should be placed with short and wide traces as near as possible to CH7517. For optimum performance, this signal should not overlay the analog power or analog output signals.

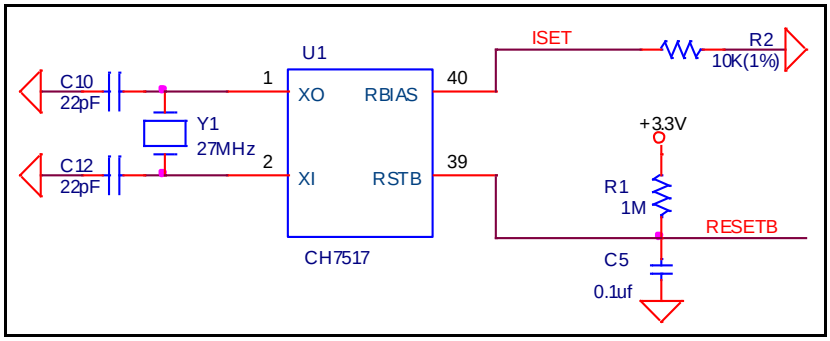

Figure 4: RBIAS Pin Connection and General Control

2.4 General Control Pins

• XI, XO

27MHz crystal can be connected to these pins of XI, XO as the CH7517 optional reference clock input. In PCB design, 27MHz crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7517, it is very important that noise should not couple into these input pins.

The crystal load capacitance, CL, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors, **Figure 4** shows a reference design for crystal circuit design.

• Reference Crystal Oscillator

CH7517 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7517. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±100 ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±100 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7517 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
C_{ext} = external load capacitance required on XI and XO pins.
C_L = crystal load capacitance specified by crystal manufacturer.
C_{int} = capacitance internal to CH7517 (approximately 10~15 pF on each of XI and XO pins).
C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that $C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int}=2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

2.5 Serial Port Control Pins

• SPC0 and SPD0

SPC0 and SPD0 function as a serial interface where SPD0 is bi-directional data and SPC0 is an input only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to AVCC (+3.3V) with 6.8kΩ resistors as shown in **Figure 5**. The 22pf capacitor can be used to decrease noise interference. Through these two pins, the firmware can be upgrade into the internal flash memory. If not used in design, they can be either pulled high or pull low with the resistors. SPC0 and SPD0 also can be connected to PIN4 (SPC0) and PIN11 (SPD0) of VGA connecter separately for firmware upgrade.

• VGA_SCL and VGA_SDA

VGA_SCL and VGA_SDA are used to interface with the DDC of VGA monitor. This DDC pair needs to be pulled up to 5V through 10K resistors as shown in **Figure 5**. A low instantaneous forward voltage diode is used to avoid back drive current from VGA monitor.

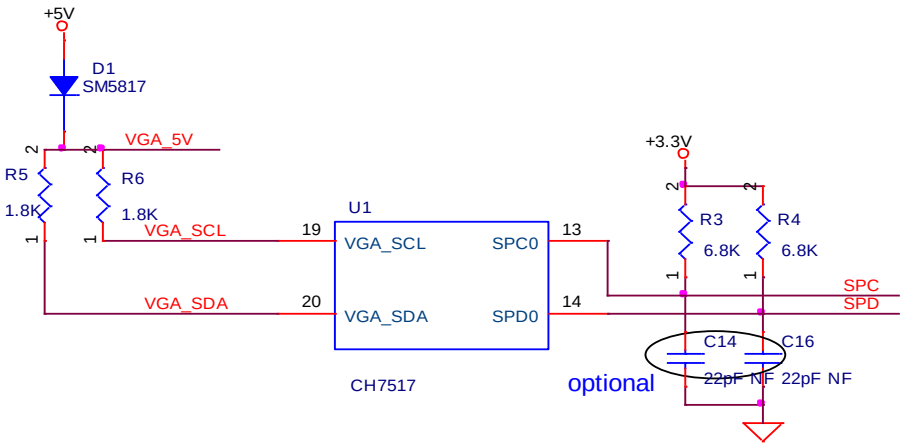

Figure 2 Serial Port Interface

2.6 Display Port Signal Pins

• DP0P/N, DP1P/N

These pins accept two AC-coupled differential pair signals from the DisplayPort transmitter.

Since the digital serial data of the CH7517 may be toggled at speeds up to 2.7 GHz, it is strongly recommended that the connection of these video signals between the graphics controller and the CH7517 should be kept as short as possible and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mils traces should be used in routing these signals. There should be 7 mils spacing between each intra pair. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bend which is smaller than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the source, as shown in **Figure 6**.

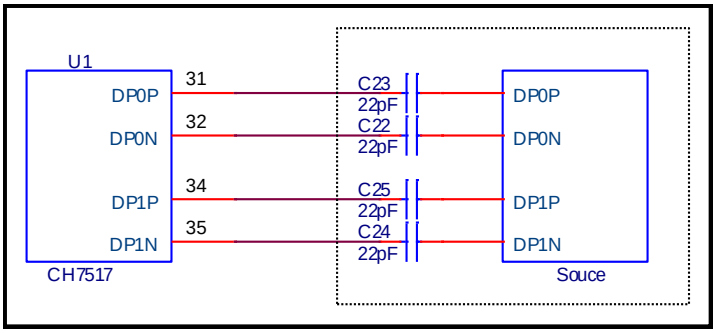

Figure 3: CH7517 DP Main Link Lane Inputs

• AUXP and AUXN

These two pins are DisplayPort AUX channel control that accepts a half-duplex, bi-directional AC-coupled differential signal.

They must have the AC-coupling capacitors, and 100nF capacitors are recommended in this document, as shown in **Figure 7**.

• HPD

This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3V. A resistor more than 100K-Ohm should be connected between this pin and GND, as shown in **Figure 7**.

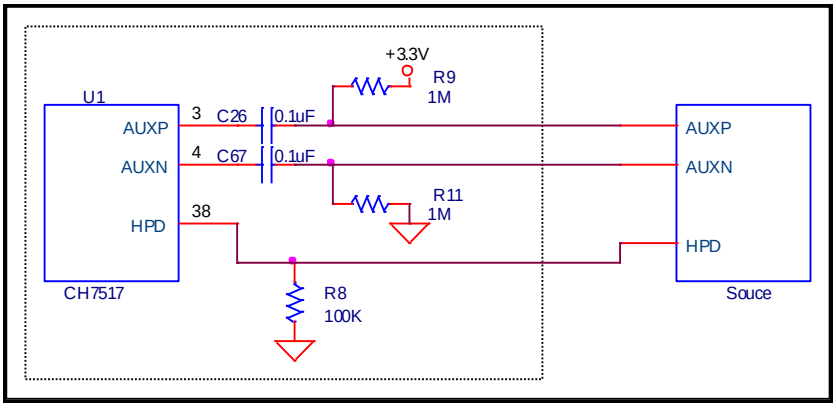

Figure 4: CH7517 AUX channel and HPD

2.7 VGA Output Pins

• RDAC, GDAC and BDAC

Three on-chip 9-bit high speed DACs provide RGB output. If the DACs require a double termination, a 75 Ω resistor should be placed between each DAC pin and the ground as shown in **Figure 8**.

• HSO and VSO

The HSO and VSO are COMS output Pins, The voltage level is the same with AVCC.

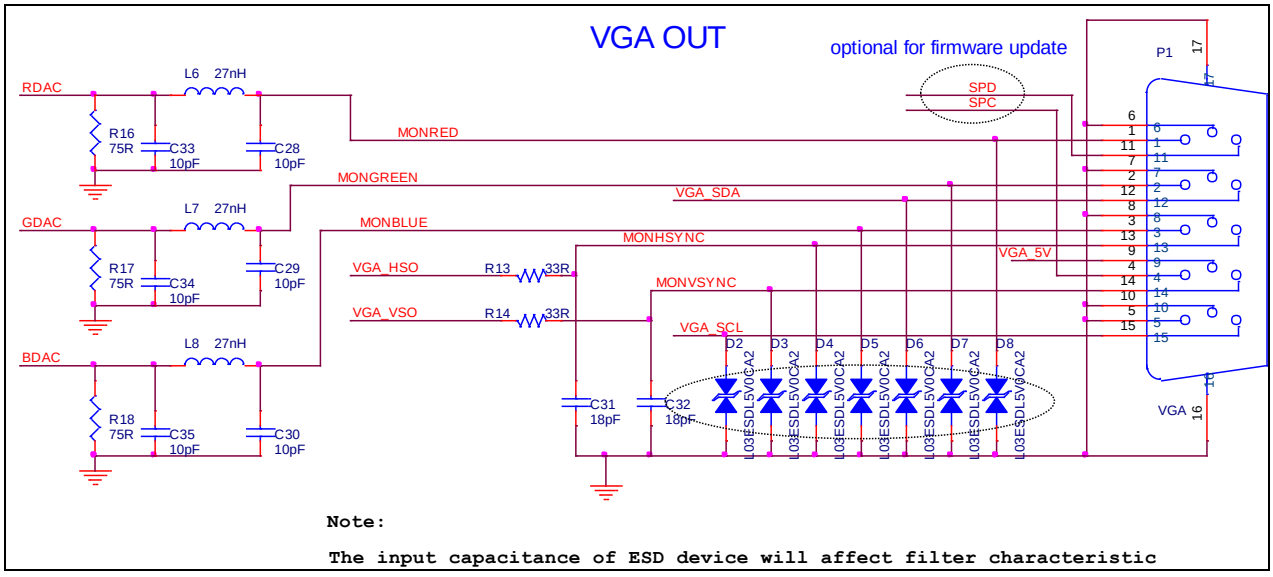

Figure 5: The CH7517 VGA outputs

2.8 Thermal Exposed Pad Package

The CH7517 is available in 40-pin QFN package with thermal exposed pad package. The advantage of the thermal exposed pad package is that the heat can be dissipated through the ground layer of the PCB more efficiently. When properly implemented, the exposed pad package provides a means of reducing the thermal resistance of the CH7517.

Careful attention to the design of the PCB layout is required for good thermal performance. For maximum heat dissipation, the exposed pad of the package should be soldered to the PCB as shown in **Figure 9.**

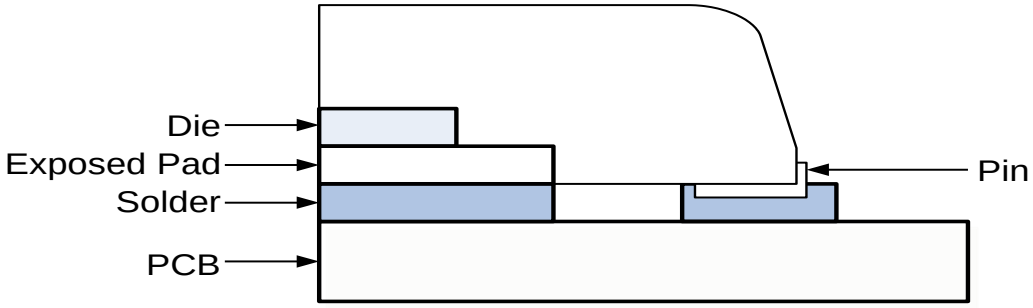

Figure 6: Cross-section of exposed pad package

3.0 REFERENCE DESIGN EXAMPLE

The following schematics are to be used as a CH7517 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7517 and would like to have a complete reference design schematic, which should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example

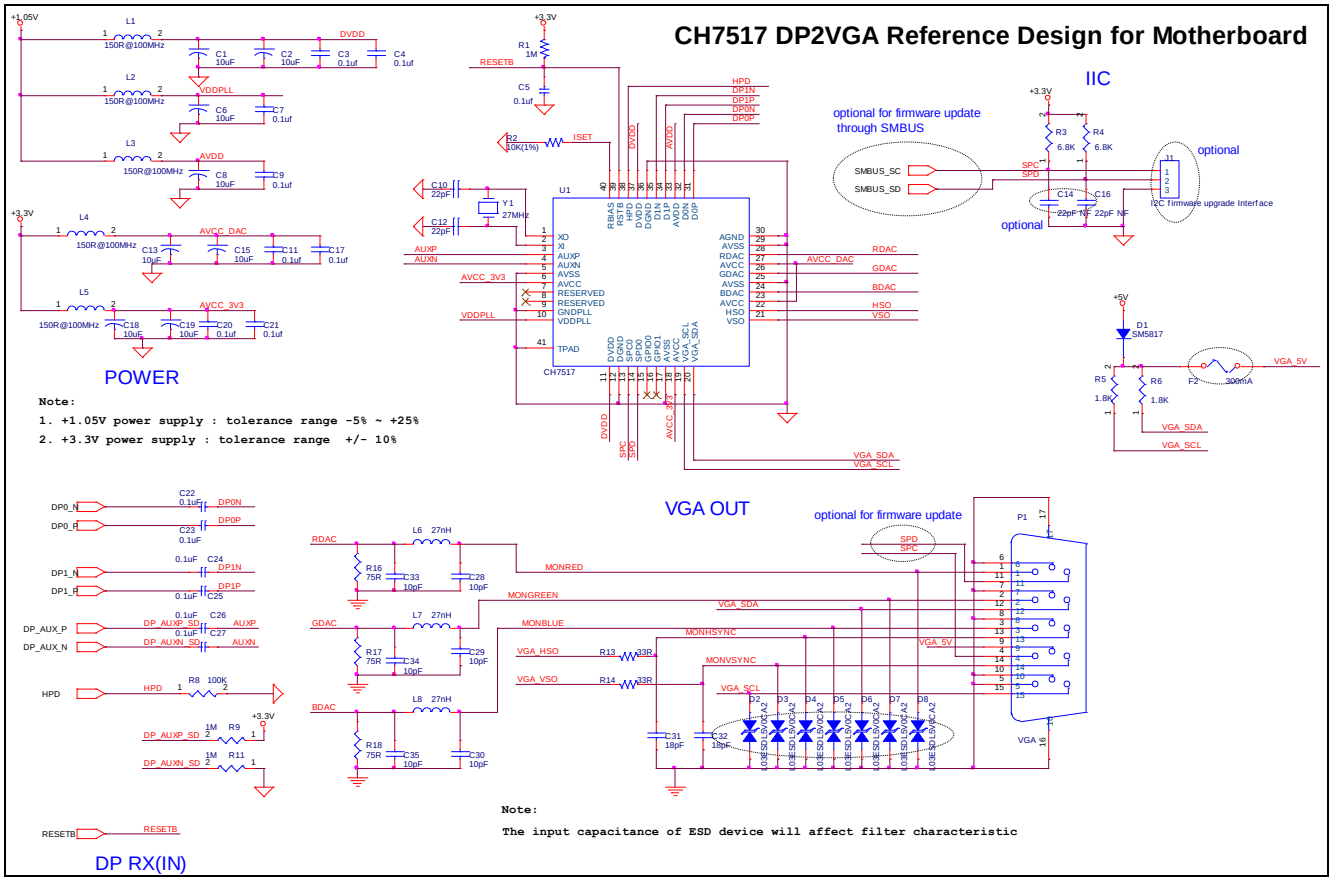

Figure 10: CH7517 Reference schematic

3.2 Reference Board Preliminary BOM

Table 2: CH7517 Reference Design BOM List

Item	Quantity	Reference	Part
1	8	C1,C2,C6,C8,C13,C15,C18,	10uF
		C19	
2	15	C3,C4,C5,C7,C9,C11,C17,	0.1uf
		C20,C21,C22,C23,C24,C25,	
		C26, C27	
3	4	C10, C12, C14,C16	22pF
4	6	C28, C29, C30,C33,C34,C35	10pF
5	2	C31, C32	18pF
6	1	D1	SM5817
7	7	D2,D3,D4,D5,D6,D7,D8	L03ESDL5V0CA2
8	1	F2	Fuse 300mA
9	5	L1,L2,L3,L4,L5	FB (150R@100MHz)

10	3	L6, L7, L8	47nH
11	1	P1	VGA connector
12	2	R13,R14	33R
13	3	R1,R9,R11	1M
14	1	R2	10K(1%)
15	2	R3,R4	6.8K
16	2	R5,R6	1.8K
17	3	R16,R17,R18	75R
18	1	R8	100K
19	1	U1	CH7517
20	1	Y1	27MHz

4.0 REVISION HISTORY

Table 3: Revisions

Rev. #	Date	Section	Description	Internal Use only(rev)
0.1	2012/10/31	all	Create	
0.5	2012/11/09	2.6, 3	Modify VGA DAC filter	
0.6	2012/11/16	2.6, 3	Modify VS, HS filter	
		2.3	Add Reference Crystal Oscillator description	
		2.3	Add power on reset description	
0.7	2013/08/02	2.4,3	Change VGA DDC pull-up resistor.	
0.8	2013/11/13	2.6, 3	Modify VGA DAC filter	
0.9	2013/11/20	3	Modify IIC slave	
1.0	2013/12/13	2.6, 3	Modify VGA DAC filter	
1.1	2017/04/27	2.2, 2.3	Add power on and off description	
1.2	2019/05/06	2.2	Update the Power-on sequnce	
1.3	2020/07/15	Disclaimer	Update the Disclaimer	

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